

# PHP/PHB110NQ08LT

N-channel TrenchMOS™ logic level FET

Rev. 01 — 29 March 2004

Product data

## 1. Product profile

### 1.1 Description

Logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Logic level threshold
- Very low on-state resistance.

### 1.3 Applications

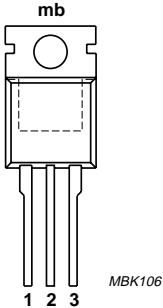
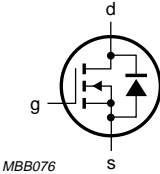
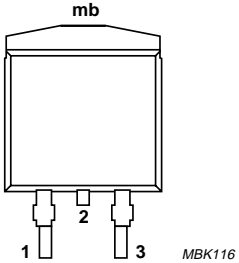
- Motors, lamps, solenoids
- DC-to-DC converters
- Uninterruptible power supplies
- General industrial applications.

### 1.4 Quick reference data

- $V_{DS} \leq 75$  V
- $I_D \leq 75$  A
- $P_{tot} \leq 230$  W
- $R_{DSon} \leq 8.5$  m $\Omega$ .

## 2. Pinning information

Table 1: Pinning - SOT78 (TO-220AB) and SOT404 (D<sup>2</sup>-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) <span style="color: red;">[1]</span>		
3	source (s)		
mb	mounting base; connected to drain (d)		
		SOT78 (TO-220AB)	SOT404 (D <sup>2</sup> -PAK)

[1] It is not possible to make connection to pin 2 of the SOT404 package.



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### 3. Ordering information

Table 2: Ordering information

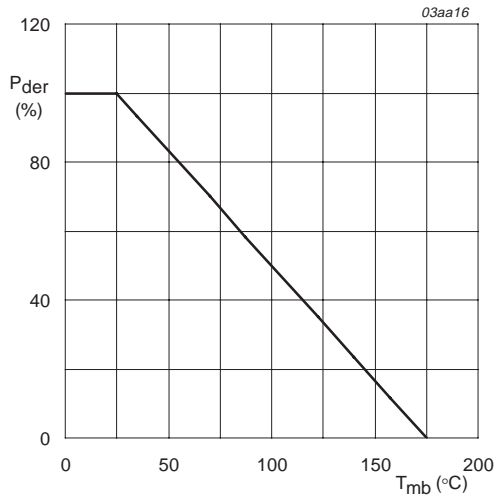
Type number	Package		Version
	Name	Description	
PHP110NQ08LT	TO-220AB	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads	SOT78
PHB110NQ08LT	D <sup>2</sup> -PAK	Plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT404

### 4. Limiting values

Table 3: Limiting values

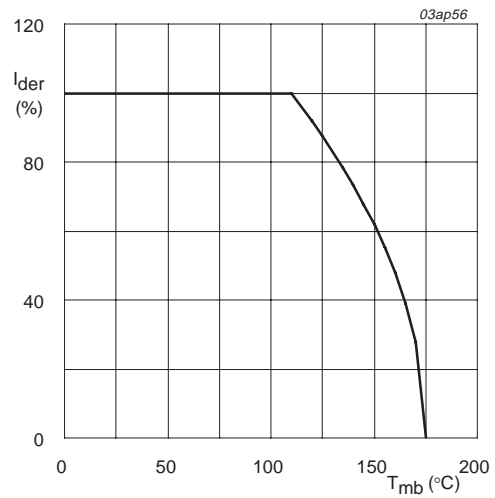
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	75	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	75	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 20$	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2 and 3</b>	-	75	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2</b>	-	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <b>Figure 3</b>	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <b>Figure 1</b>	-	230	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	75	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	240	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75\text{ A}$ ; $t_p = 0.15\text{ ms}$ ; $V_{DD} \leq 75\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; starting $T_j = 25\text{ °C}$	-	560	mJ



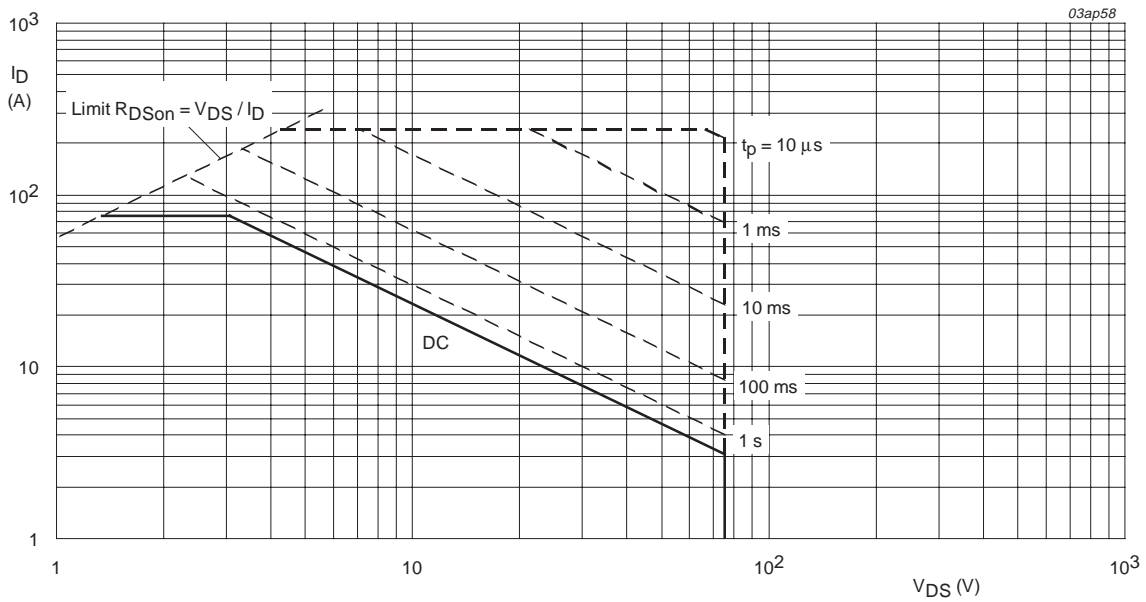
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^\circ C$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 10 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

### 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.65	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT404	mounted on printed-circuit board; minimum footprint; vertical in still air.	-	50	-	K/W

#### 5.1 Transient thermal impedance

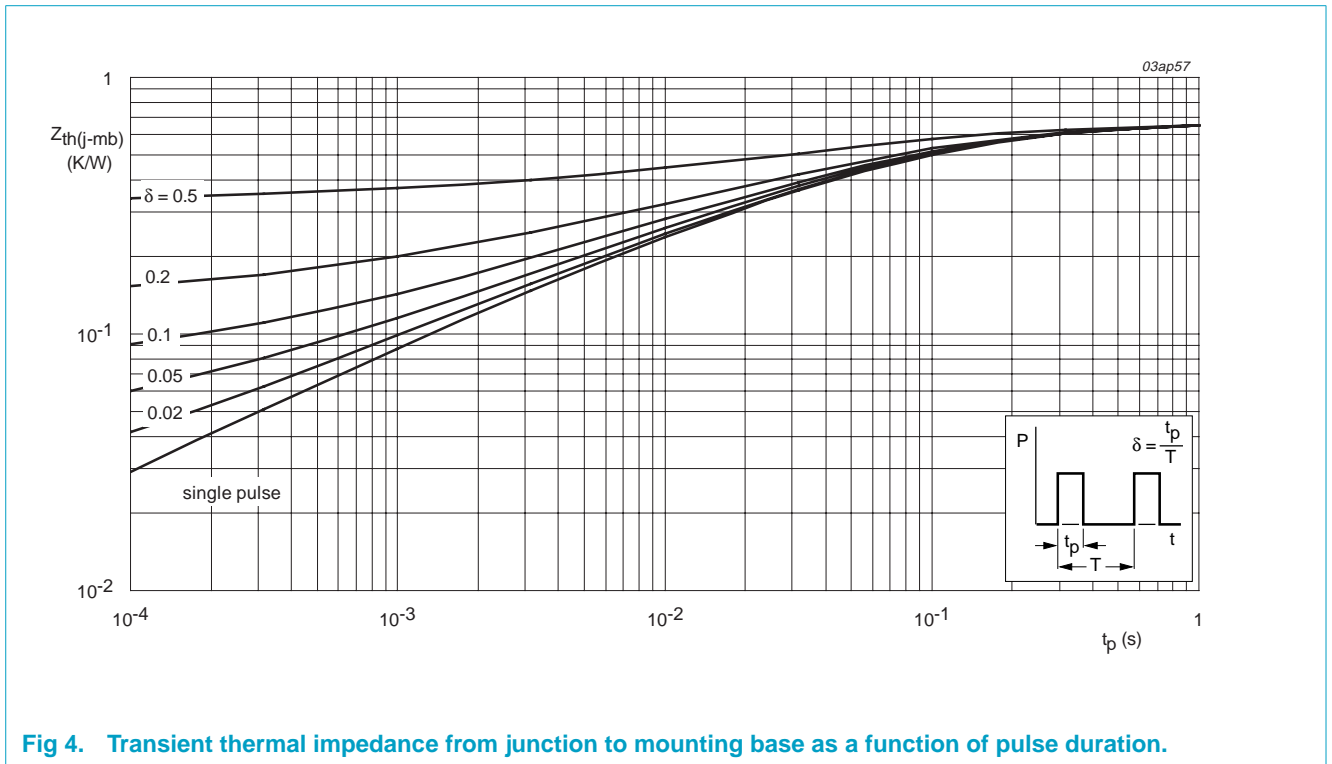
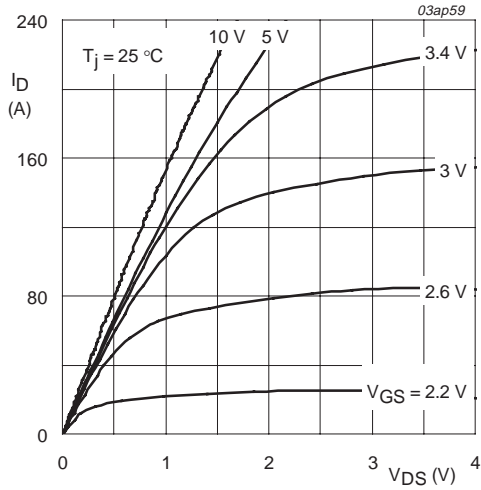


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 6. Characteristics

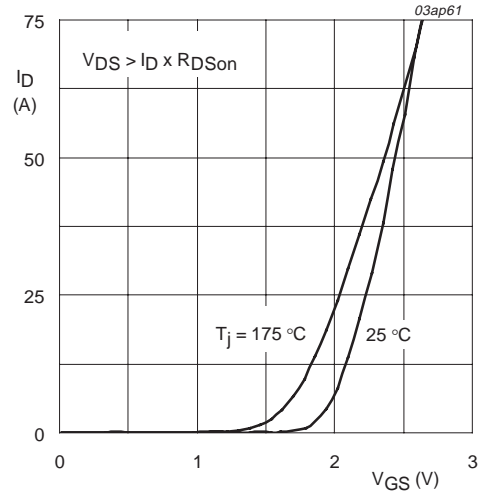
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	75	-	-	V
		T <sub>j</sub> = -55 °C	70	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <b>Figure 9</b> T <sub>j</sub> = 25 °C	1	1.5	2	V
		T <sub>j</sub> = 175 °C	0.5	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.2	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 75 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	-	-	10	μA
		T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±10 V; V <sub>DS</sub> = 0 V	-	2	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; <b>Figure 7 and 8</b> T <sub>j</sub> = 25 °C	-	7.2	8.5	mΩ
		T <sub>j</sub> = 175 °C	-	15.1	17.9	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; <b>Figure 7 and 8</b>	-	7.6	9	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; <b>Figure 8</b>	-	-	9.95	mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DD</sub> = 60 V; V <sub>GS</sub> = 10 V; <b>Figure 13</b>	-	127.3	-	nC
Q <sub>gs</sub>	gate-source charge		-	12.5	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	54.5	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; <b>Figure 11</b>	-	6631	-	pF
C <sub>oss</sub>	output capacitance		-	905	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	610	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 30 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 5 V; R <sub>G</sub> = 10 Ω	-	47	-	ns
t <sub>r</sub>	rise time		-	185	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	424	-	ns
t <sub>f</sub>	fall time		-	226	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; <b>Figure 12</b>	-	0.77	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V	-	70	-	ns
Q <sub>r</sub>	recovered charge		-	213	-	nC



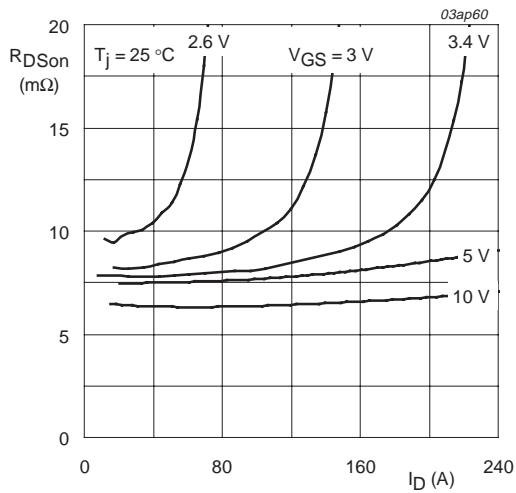
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



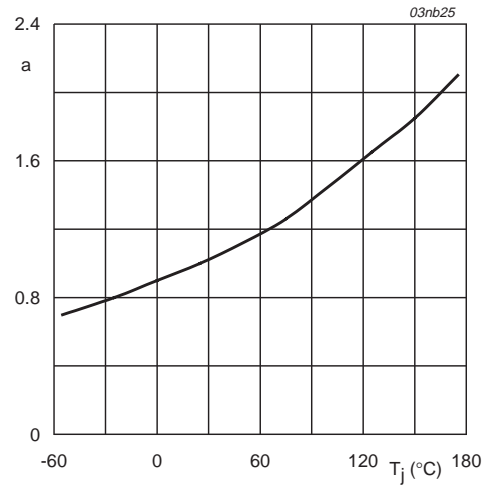
$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



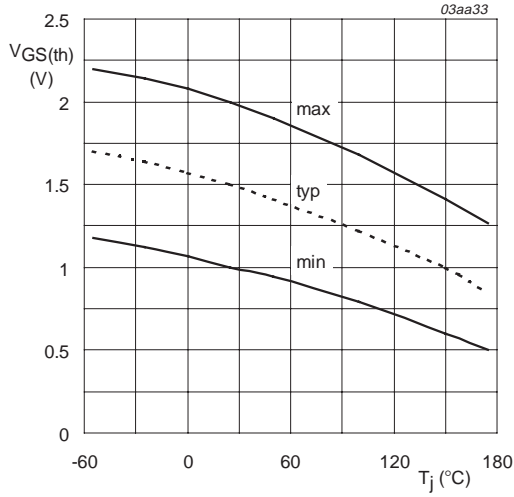
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



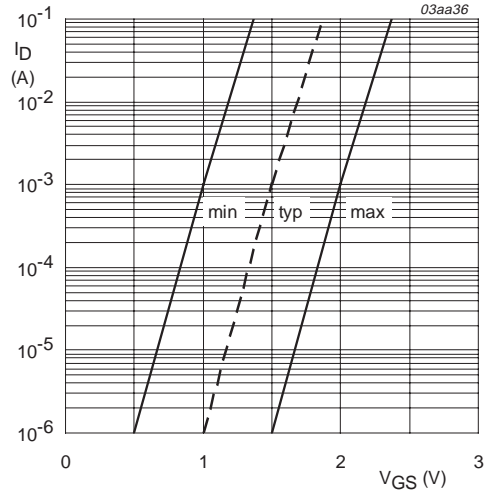
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



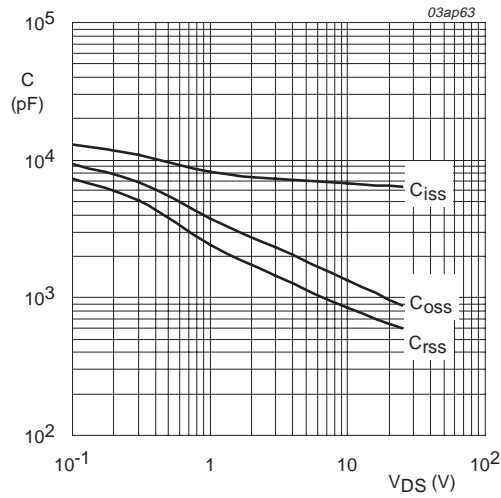
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



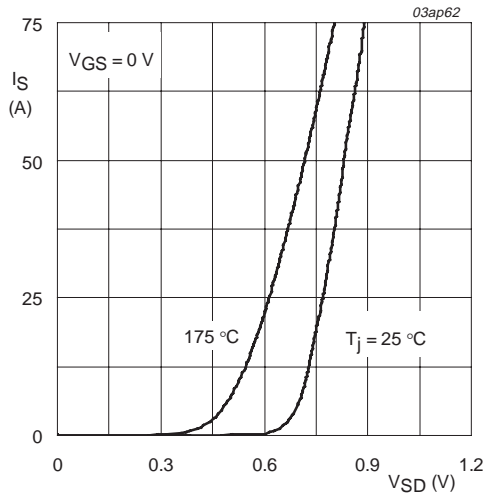
$T_J = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



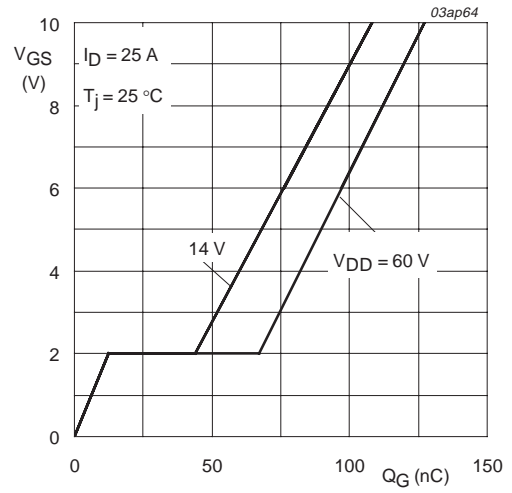
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$  and  $175\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 25\text{ A}$ ;  $V_{DD} = 14\text{ V}$  and  $60\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**



7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



Fig 14. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404

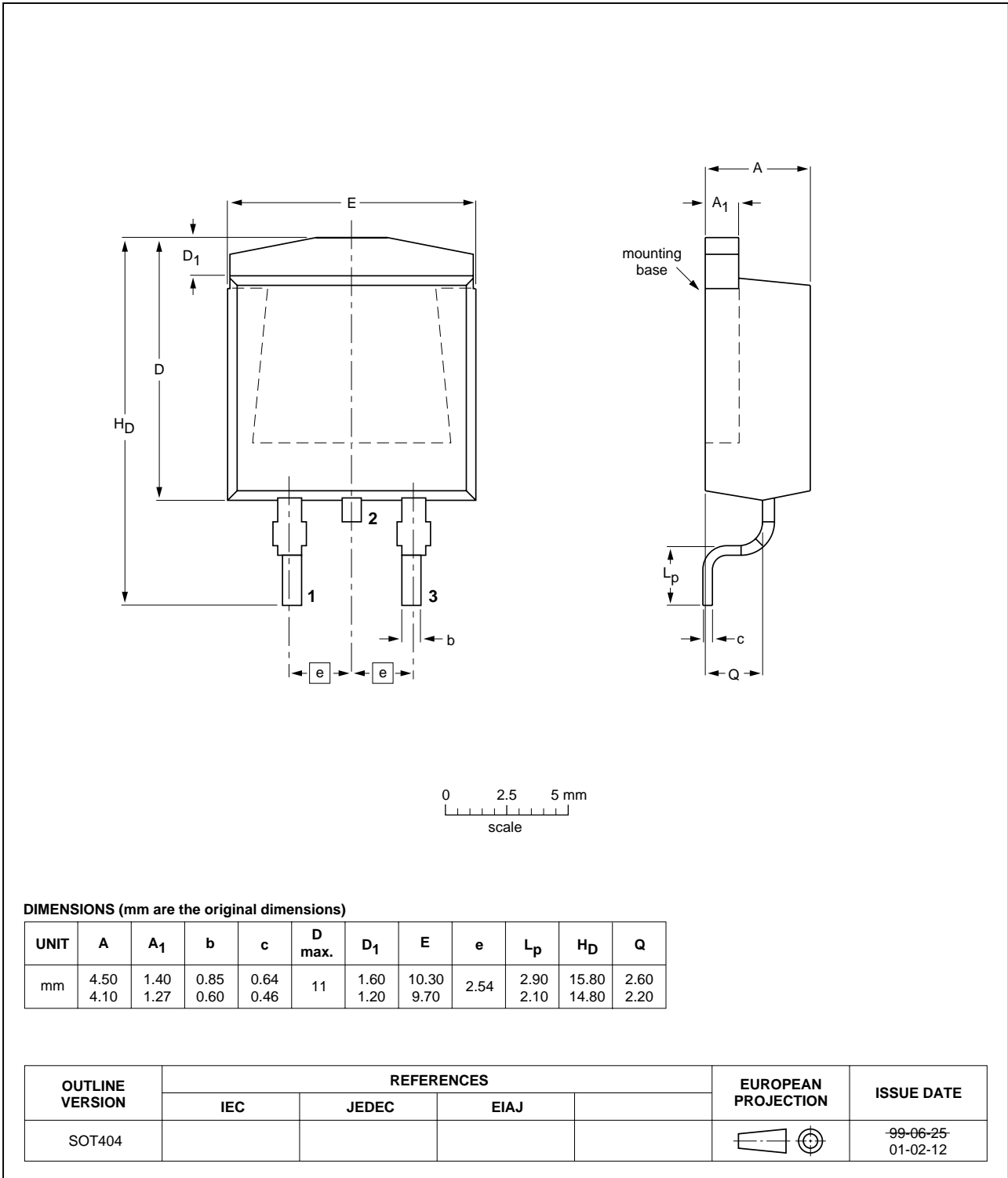


Fig 15. SOT404 (D<sup>2</sup>-PAK).

## 8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040329	-	Product data (9397 750 12924)

## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

Fax: +31 40 27 24825

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